PVP 20

Code: 20EE3301, 20EC3301

II B.Tech - I Semester – Regular Examinations - FEBRUARY 2022

ELECTRONIC DEVICES AND AMPLIFIER CIRCUITS

(Common for EEE, ECE)

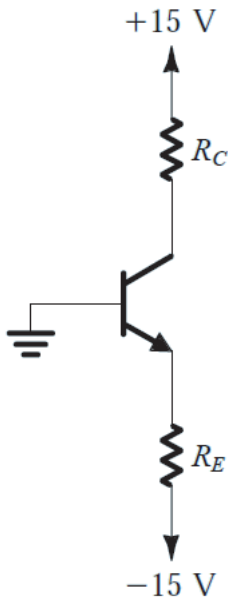
Duration: 3 hours Max. Marks: 70

Note: 1. This paper contains questions from 5 units of Syllabus. Each unit carries 14 marks and have an internal choice of Questions.
2. All parts of Question must be answered in one place.

UNIT – I

1. a) With a circuit diagram, illustrate the operation of a common emitter amplifier and obtain its voltage gain expression. 7 M

   b) Design a circuit similar to that shown in below figure except that now the power supplies are ± 1.5V and the BJT has β =100 and exhibits V_{BE} of 0.8V at i_c=1mA. Design the circuit so that a current of 2 mA flows through the collector and a voltage of +5V appears at the collector. 7 M



OR

2. a) Compare common base (CB), common emitter (CE) and common collector (CC) configuration of a transistor. For CE configuration prove that $I_C = \beta I_B + (\beta+1)I_{CO}$ — 7 M

   b) For a CE transistor amplifier circuit, R_1=50KΩ, R_2=25KΩ, R_C=10KΩ, R_E=10KΩ, R_L=30KΩ. Determine input and output impedances, current gain and voltage gain if transistor parameters are as follows h_{ie}=2KΩ, h_{fe}=100, h_{re}=5x10^{-4} , h_{oe}=25μS. — 7 M

UNIT – II

3. a) Analyze the MOSFET biasing technique using a large drain-to-gate feedback resistance R_G. Design the drain-to-gate feedback biasing circuit to operate at a DC drain current of 0.5mA. Assume V_{DD} =5V, k_n'W/L=1mA/V^2, λ=0. — 7 M

   b) What are the main constructional differences between a MOSFET and a BJT? What effect do they have on the current conduction mechanism of a MOSFET? — 7 M

OR

4. a) With neat diagram analyze the operation of MOSFET in depletion mode and derive its current equations. — 7 M

   b) Differentiate between current voltage relationships of the N channel and P channel MOSFET. — 7 M

UNIT-III

5. a) Obtain the expression for low frequency response of a MOSFET common source amplifier. — 7 M

b) A MOSFET is to operate at I_D=0.1mA and is to have g_m=1mA/V. If k_n= 50μA/V^2. Estimate the required W/L ratio and the overdrive voltage. 7 M

OR

6. a) Analyze the internal capacitances of a MOSFET and hence draw the high frequency model of MOSFET. 7 M

b) Estimate the mid band gain A_M, and the upper 3-dB frequency f_H of a MOSFET CS amplifier fed with a signal source having an internal resistance R_{sig}=100 kΩ. The amplifier has R_G=4.7M**Ω**, R_D=R_L=15kΩ, , g_m=1mA/V, r_o=150k**Ω** , C_{gs}=1pF and C_{gd}=0.4pF 7 M

UNIT – IV

7. a) Explain the MOS differential pair with common mode input voltage and specify the input common mode voltage range. 7 M

b) Show that if all transistors are operated at an overdrive voltage V_{ov} and have equal Early voltages $|V_A|$, the gain is given by $A_d = 2(V_A/V_{oV})^2$. Estimate the gain for V_{ov}= 0.25 V and V_A = 20 V. 7 M

OR

8. a) Obtain input offset voltage of the MOS differential pair with necessary diagrams. 7 M

b) An NMOS differential amplifier utilizes a bias current of 200 μA. The device have V_t =0.8V, W=100 μm, and L=1.6 μm, in a technology for which $\mu_n C_{ox}$= 90 μA/V^2. Find V_{GS}, g_m and the value of V_{id} for full-current switching. To what value should the bias current be changed in order to double the value of V_{id} for full- 7 M

current switching?

UNIT – V

9. a) Compare the operating regions of Bipolar and MOS transistors. 7 M

   b) Interpret the current steering circuit using five MOSFET transistors and distinguish the current source and current mirror. 7 M

OR

10. a) Explain the operation of MOS current steering circuit and mention its advantages. 7 M

    b) Show that for a MOSFET the selection of L and V_{ov} determines A_0 and f_T. In other words, show that A_0 and f_T will not depend on I_D and W. 7 M